In the Claims.

1. (Amended) A semiconductor integrated circuit device, comprising:

a plurality of insulated gate field effect transistors IGFETs coupled to a corresponding input/output (I/O) terminal through a corresponding first resistance;

a first clamping device coupled to each I/O terminal;

a second clamping circuit corresponding to each IGFET, each second clamping circuit including a second clamping device and the corresponding first resistance, each second clamping device having a first terminal connected to a gate electrode of the corresponding IGFET and a second terminal connected to a source/drain terminal of the corresponding IGFET and a supply potential wiring;

each first clamping device being coupled to one second clamping device through a second resistance; and

at least two of the second clamping circuits vary from one another.

16. (Amended) A method for designing a protective circuit for a semiconductor integrated circuit device that includes insulated gate field effect transistors IGFETs formed thereon, the method comprising the steps of:

executing a simulation with a predetermined charged device model (CDM) equivalent circuit that includes a first clamping device connected to an input/output (I/O) terminal, a first IGFET having a gate connected to the I/O terminal through a first resistance (Rin), a second clamping device connected between gate and source/drain terminals of the first IGFET and connected to a supply potential wiring, the first and second clamping devices being connected to one another through a second resistance (Rg); and

selecting a ratio of the second resistance and the first resistance (Rg/Rin) that prevents a potential between the gate and source/drain terminal of the first IGFET from exceeding a predetermined value.